Characteristics of Monolithically Integrated InGaAs Active Pixel Imager Array

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ABSTRACT

Switching and amplifying characteristics of a newly developed monolithic InGaAs Active Pixel Imager Array are presented. The sensor array is fabricated from InGaAs material epitaxially deposited on an InP substrate. It consists of an InGaAs photodiode connected to InP depletion-mode junction field effect transistors (JFETs) for low leakage, low power, and fast control of circuit signal amplifying, buffering, selection, and reset. This monolithically integrated active pixel sensor configuration eliminates the need for hybridization with silicon multiplexer. In addition, the configuration allows the sensor to be front illuminated, making it sensitive to visible as well as near infrared signal radiation. Adapting the existing 1.55 µm fiber optical communication technology, this integration will be an ideal system of optoelectronic integration for dual band (Visible/IR) applications near room temperature, for use in atmospheric gas sensing in space, and for target identification on earth. In this paper, two different types of small 4x1 test arrays will be described. The effectiveness of switching and amplifying circuits will be discussed in terms of circuit effectiveness (leakage, operating frequency, and temperature) in preparation for the second phase demonstration of integrated, two-dimensional monolithic InGaAs active pixel sensor arrays for applications in transportable shipboard surveillance, night vision, and emission spectroscopy.

Keywords: Dual (Visible/IR) responses, Active pixel sensor (APS), InGaAs, InP imaging detector.

1.   INTRODUCTION

Continued efforts to combine the InGaAs PIN photodiode detector technology on InP substrate with the InP JFET technology[1-2] were made. The monolithically integrated sensor array with active pixel readout technology has been recognized as the future space mission technology of a miniaturized smart imaging system. This array eliminates the need for hybridization with a separate silicon readout chip. The Jet Propulsion Laboratory has been working with Sensors Unlimited of Princeton, New Jersey to produce such a sensor for a low leakage, low power mobile imaging system. This monolithic sensor array is front-illuminated, providing near-IR to visible response. It largely eliminates the problem of the high charge transfer efficiency, allowing the construction of large yet highly reliable Infrared focal plane arrays (IR FPAs). It can make use of high electron mobility at near room temperature inherent in InP JFETs to enable readout speeds unobtainable in a silicon readout.

IR FPAs have a wide range of industrial, scientific, and military applications.[3, 4] In general, an IR FPA consists of an array of infrared-sensitive photodetectors and associated readout electronics capable of converting, amplifying, buffering and multiplexing the signal charge from detector arrays. In a typical IR FPA array, the detector is fabricated from a narrower bandgap film in a III-V or II-VI material. For example InGaAs is epitaxially deposited on the front surface of a wider bandgap substrate, such as InP. This diode array chip is then "flipped" and bump-bonded with the patterned surface down, and the substrate up to a separate readout chip. This readout chip is almost always formed from silicon CMOS because of the high maturity of this silicon technology. Silicon circuits of great complexity can easily be designed and simulated since highly sophisticated design tools are available for this purpose. Commercial foundries are available to produce the chips at a relatively low cost with high yield. This hybrid structure, consisting of a diode array chip bump-bonded to a silicon CMOS readout, has worked well and has been exploited in IR FPAs spanning the wavelength ranges from 100 to 1 μm.

However, this approach is not without its problems, and there is a need to explore alternatives. First, the hybridization adds steps to the sensor fabrication sequence that are expensive and sometimes challenging. Second, the coefficient of thermal expansion (CTE) of silicon is anomalous with respect to virtually every other semiconducting materials system. Since IR FPAs usually must be cooled for optimum performance (in order to reduce dark current), this difference in CTE causes a mismatch in the thermal expansion between the detector and readout chips, straining the electrical bonds between the chips. While the use of soft indium bumps has helped accommodate this strain, the CTE mismatch limits array sizes and reduces reliability, if thermal cycling is involved.

Perhaps more importantly, the standard hybrid approach is necessarily a back-illuminated design, and incoming optical radiation must pass through the substrate of the detector array. The bandgap of the substrate material then sets the short wavelength cut-off of the detector unless the substrate can be removed after hybridization. In sensors where removing the substrate is not cost-effective or practical, the hybrid approach severely limits the wavelength range of sensitivity.

Several developments in electro-optics have occurred that can be leveraged to take a new approach to IR-FPA structure. First, InGaAs sensors on InP substrates have been developed as an alternative to shorter wavelength HgCdTe. InGaAs provides a barrier equal to the full bandgap, as opposed to the midgap barrier in a metal gate transistor (MESFET).[5-6] This greater barrier provides a wider logic swing for digital logic as well as reduced gate leakage for analog circuits. InGaAs, with a cut-off wavelength of 1.7 μm, is lattice-matched to InP and has been used to make high quality area arrays. By using super-lattice techniques to relieve the strain due to lattice mismatch, strain relaxed detectors of pure InAs on InP have also been demonstrated. These extend the cutoff wavelength to approximately 2.5 μm. InGaAs photo-detectors with InGaAs JFETs on InP have also been developed, principally for high speed communication applications.

An active pixel image sensor of InGaAs PIN which is monolithically integrated on an InP JFET was described[1] elsewhere as an image sensor that has one or more active transistors within the pixel unit cell. This is in contrast to a passive pixel approach that uses a simple switch to connect the pixel signal charge to the column bus capacitance. Active pixel sensors have demonstrated lower noise readout, improved scalability to large array formats, and higher speed readout compared to passive pixel sensors. In order to utilize these advantages of the active pixel sensors however, the technology should be further improved in its stability of the circuits as well as its fill factors prior to its application to space mission systems.

In this paper, we examine the reliability of the monolithically integrated InGaAs PIN diode sensor array with InP JFETs readout electronics. Individual discrete devices (the InGaAs PIN photodiodes and InP JFETs) have been redesigned, fabricated and characterized for improvement of the pixel fill factor. These were followed by the development of prototype test cells consisting of the readout electronics for a single pixel. Very small prototype arrays (1x4 and 4x4 format) have been made by combining cells, using integrated select transistors to allow multiplexing. The switching stability of these sensors is discussed relating to the profile of the zinc diffused p$^+$ gate layer. The success of the metal contact covering InP PIN mesa photodiodes to the switching JFETs is described in terms of the fabrication technology of planarizing of the polyimide over the PIN mesa structure prior to the processes of gold plating and ion milling.

2. EXPERIMENTAL PROCEDURES

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Test circuits needed to construct visible and near infrared signal processing were redesigned, fabricated, and characterized using a test vector generator, a semiconductor parameter analyzer, and a lock-in amplifier. The cross-section, as shown in Figure 1, was based on InGaAs/InP PIN mesa diode of a height, 1.8 µm above the InP JFET platform level, applied for the focal plane array.[4]

A Be-doped (10^{18} cm^{-3}, thickness=400nm) p-InP JFET backing layer was grown onto the surface of (100) InP: Fe semi-insulating substrate using gas source molecular beam epitaxy. An S-doped (5×10^{16} cm^{-3}, thickness=1.0 µm) n-InP channel and contact layer (5.5×10^{17} cm^{-3}, thickness=100nm) were grown for the discrete JFET control. The n-InP contact layer was followed by a thick (1.5 µm) InGaAs detector absorption layer ($n < 1.5 \times 10^{16}$ cm^{-3}) and a thick (300nm) n-InP cap layer (2×10^{16} cm^{-3}) in succession for the completion of the PIN photodiode structure. The p$^+$-InP of the PIN photodiode contact layer and the p$^+$ isolation region around the perimeter of the JFETs were fabricated in a sealed ampoule diffusion at 500°C using Zn$_2$As$_3$ as the source. The InP n-channel was completely surrounded by p-type regions formed by a p layer under the channel and a p$^+$ wall surrounding the device perimeter. In this configuration, the depletion region pinches off the channel from both top and bottom, thereby decreasing the switching voltage by a factor of two as compared with a conventional JFET with a single gate p-n junction. There were no exposed p-n junctions.[4] Thus any surface leakage from the sidewall of the JFET mesa was eliminated.
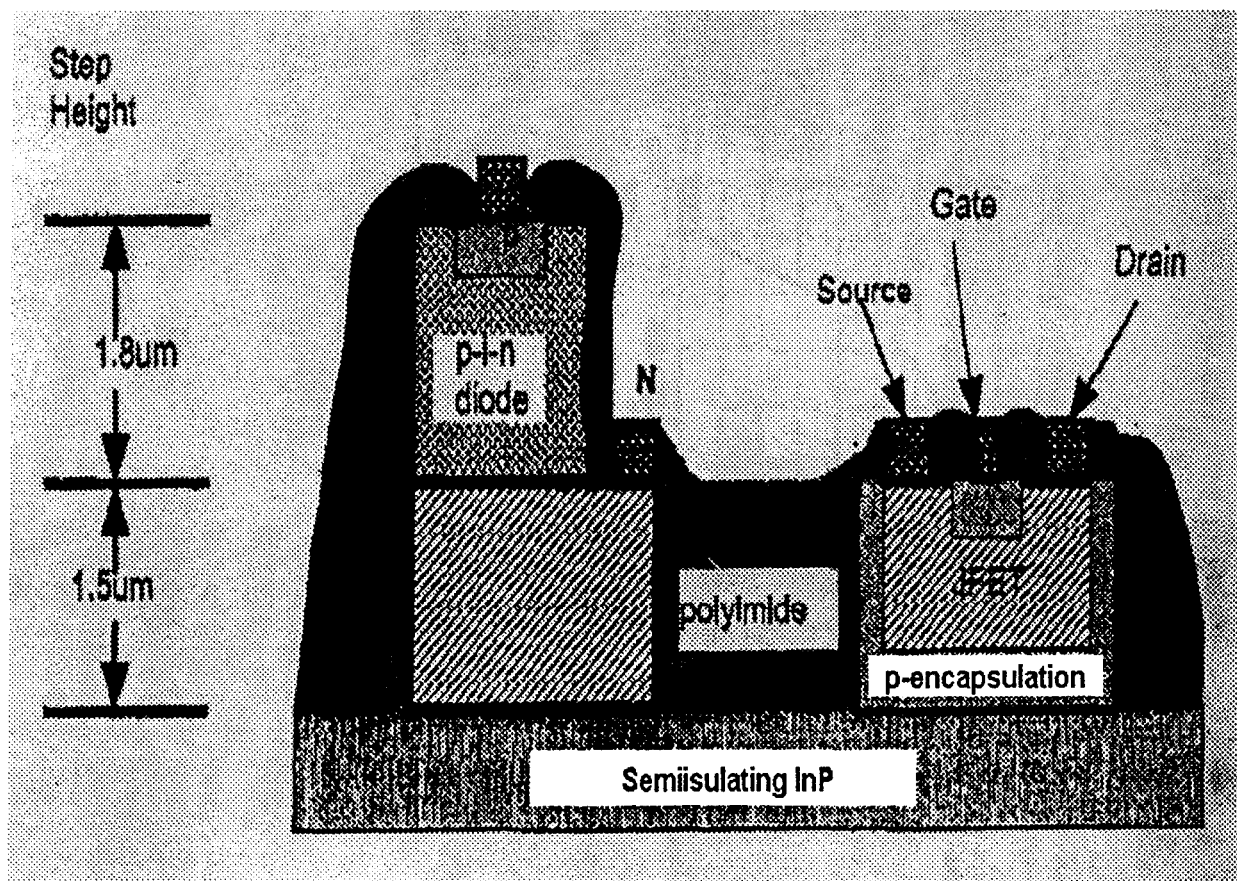

Figure 1. Cross section of the monolithically integrated InGaAs/InP PIN diode and InP junction field effect transistor platforms.
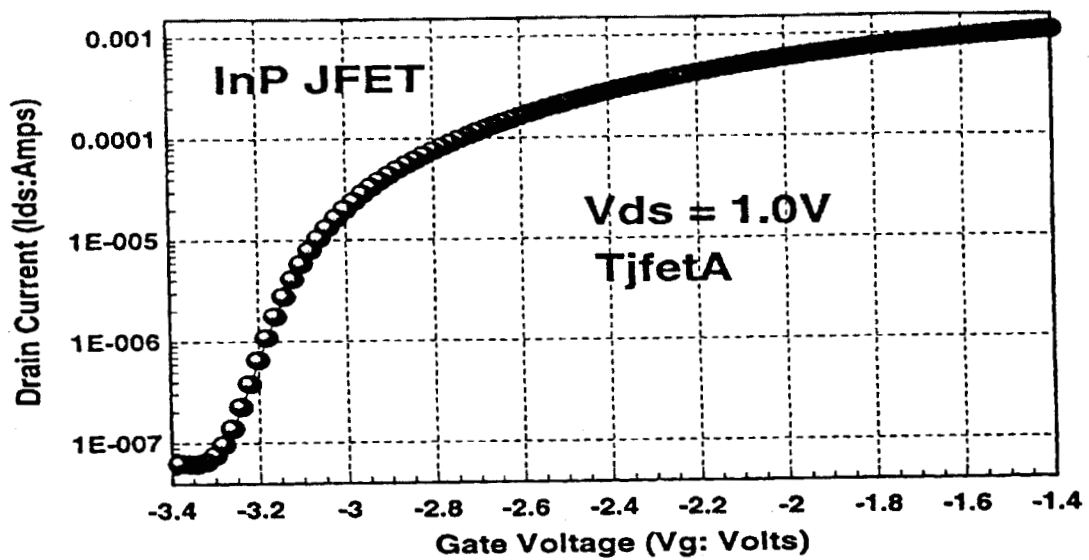
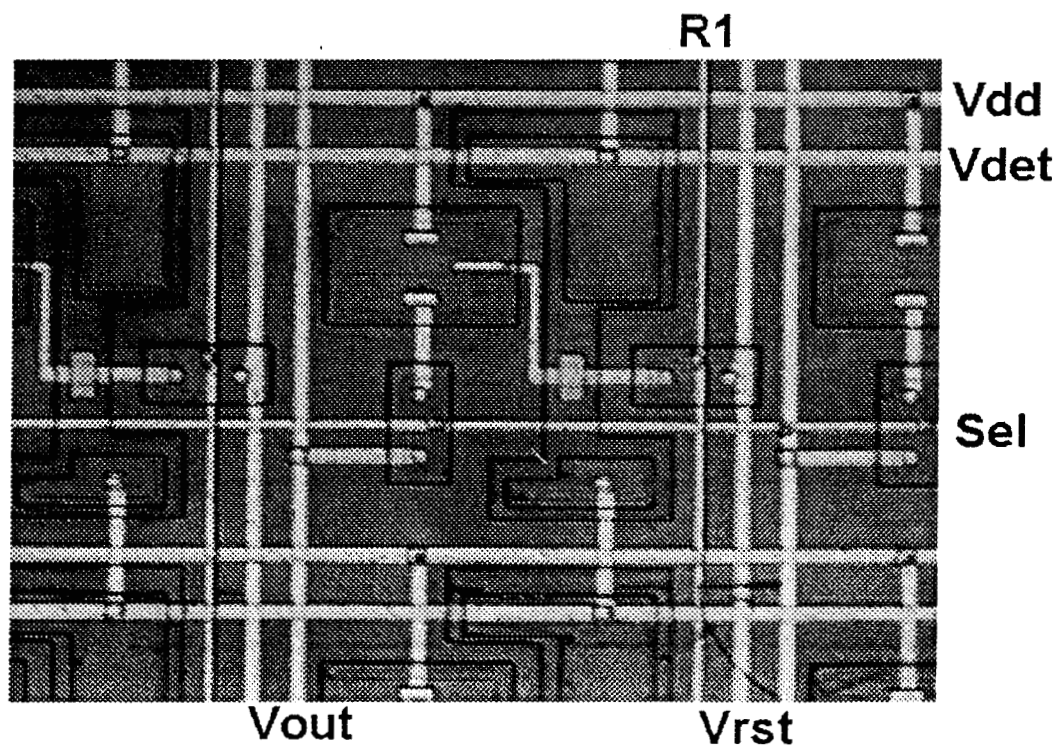Figure 2. Excellent discrete JFET Characteristics.

Figure 3. Newly designed and fabricated InGaAs PIN photodiode sensor monolithically integrated with InP JFETs for the improvement of fill factor in the Source Follower per Detector readout circuits.

3. RESULTS AND DISCUSSIONS

Figure 2 shows the typical output voltage characteristics of the newly fabricated JFETs used in amplifying signal and switching circuits in source follower per detector (SFD) readout circuits (Figure 3). *The yield of these discrete devices was excellent (>70%) in this lot.* Similar results were reported elsewhere in discrete JFETs with drain leakage current as low as 90 pA.[4] The low leakage was probably due to the pinching structures both on top of and bottom of the n-channel, the completely closed sidewalls of the p^+ isolation layers and the lightly doped n-channel InP material.
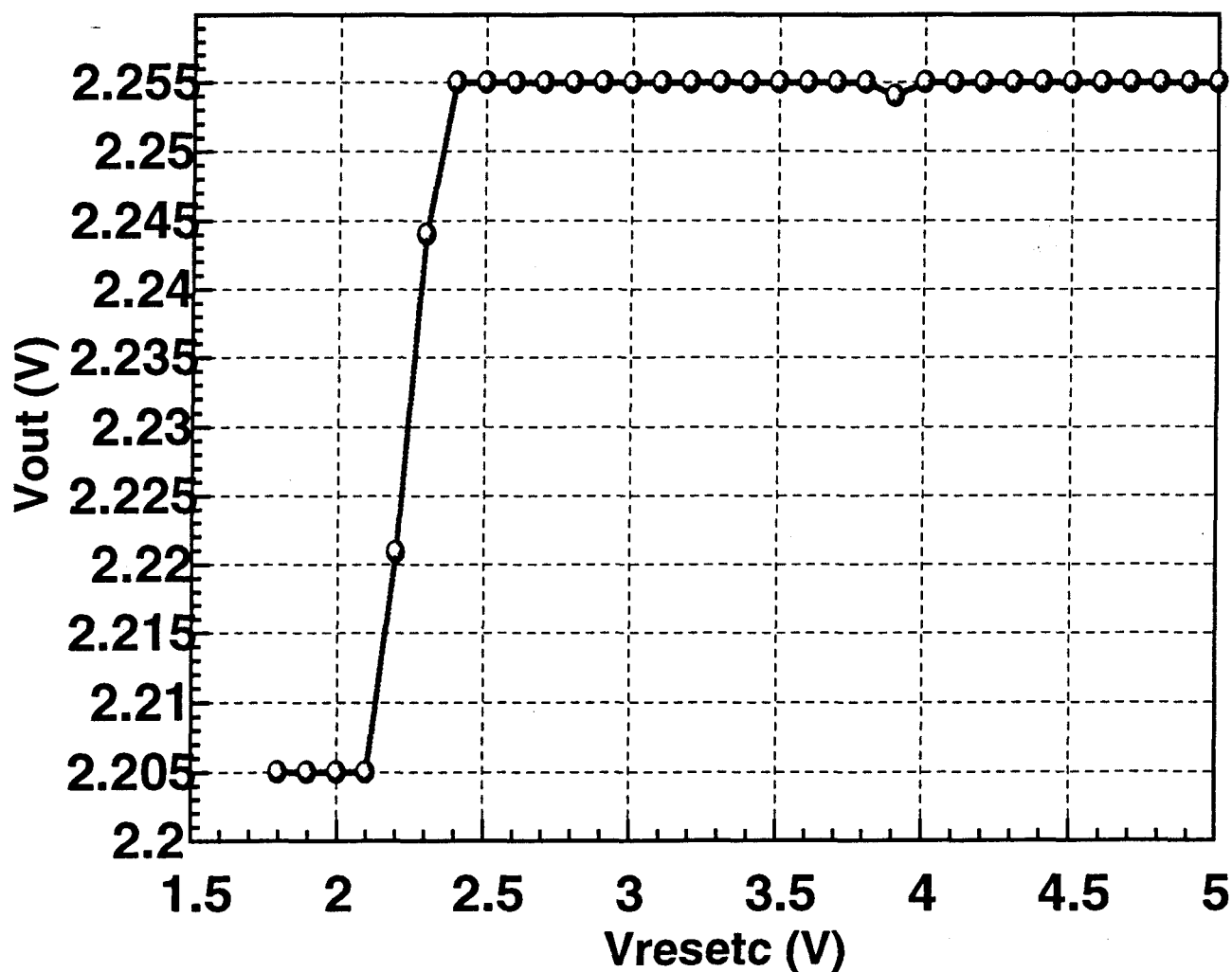
a). Voltage swing is too small.
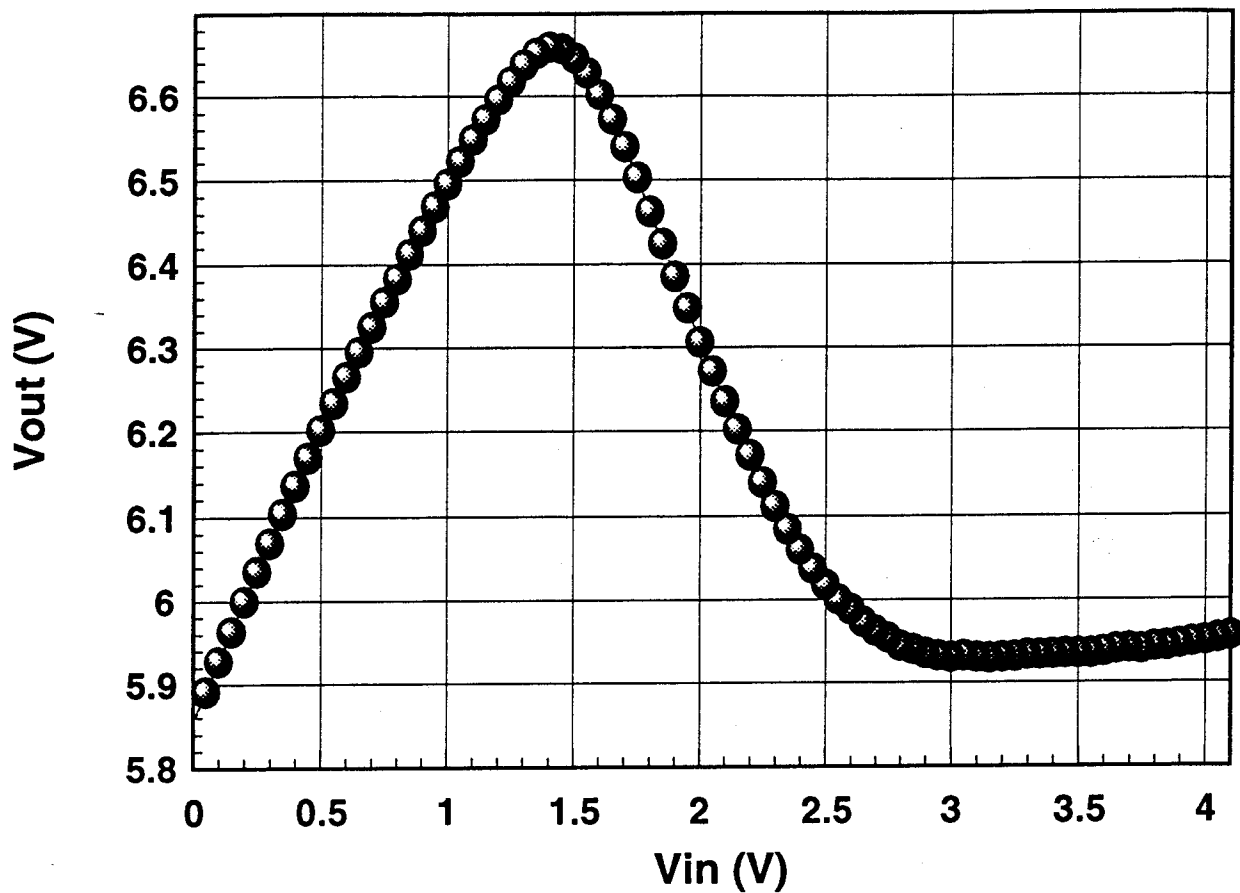
b). The leakage is too large to maintain the converted signal.

Figure 4. The switching characteristics of failed inverters of 4x1 capacitive trans-impedance amplifier (CTIA) arrays.

The switching characteristics of the source follower per detector (SFD) readout circuits are shown in Figures 4a and 4b. By changing the reset voltage control less than 0.5 V, the output voltage was sharply increased by 0.05 V reaching a maximum (Figure 4a). The detectivity of the hybrid InGaAs focal plane arrays (FPAs) was reported to be at least two orders of magnitude higher than that of the HgCdTe FPAs at room temperature. However, less than 20% of the array was functional. Furthermore, the voltage swing of some failed converters appeared to be too small to utilize the component for the readout circuits (Figure 4a). Figure 4b shows another device test result. The voltage swing of some failed was improved more than order of two (2), yet the converter leaked severely when the reset voltage reached 1.5 V. Test results indicate that the most critical variable of the successful readout circuit was the gate dopant profile. The effectiveness of p^+ diffusion was also closely dependent upon the growing technique of the multi-layers, such as molecular beam epitaxial growth or molecular beam chemical vapor deposition. Further study is on the way to improve the metallic interconnection through and on the

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4. SUMMARY

Excellent characteristics of the redesigned high fill factor InGaAs PIN integrated with JFETs SFD have been achieved for the discrete components needed to construct the monolithic InGaAs PIN/InP JFET readout circuits. Fully monolithic visible/near-infrared 1 x 4 active pixel sensors were redesigned and fabricated for the improvement of the switching action and fill factors. In this layout InGaAs photodiode detectors can be individually controllable at each pixel level by biasing the gates of InP JFETs with a minimal voltage. However, the stability of the circuit contacts should be improved further prior to the actual space applications of these sensors. The critical variable of the readout circuits appeared to be the dopant distribution of the p^+ gate layer of the JFET switch. The step formation mechanism of the p^+ gate dopants of this material was discussed in terms of diffusion element, temperature, and duration. However, the metal interconnects through and on the polyimide multilayers should be further improved to raise the device reliability.

5. FUTURE DIRECTIONS

To find a better method of connecting non-planar solid state electronic components, we looked to the work currently being used in the GaAs IC and the InP heterojunction bipolar technology. Following the path of previously developed technology, solving this interconnect problem within the relatively short time is the remaining goal for this project.

The new, proposed interconnect system improves the surface planarization of the devices and employs a plating technique for depositing the interconnects instead of using photo-lift-off. The new process proceeds as follows:[4]

1. Spin PI-2556 polyimide @5000 RPM and cure for 2 hours at 200°C.
2. Repeat step #1 two more times for a total of 3 coatings.
3. Use oxygen RIE to back-etch polyimide so it is co-planar with the top of the p-I-n mesa.
4. Perform photolithography to open via holes through the polyimide to the contact nodes.
5. Selectively etch via holes with oxygen RIE. Strip photoresist.
6. Deposit plating membrane consisting of 500A titanium and 10nm gold.
7. Perform Interconnect #1 photolithography.
8. Gold plate the interconnect metal with gold to a total thickness of 1 μm.
9. Remove photoresist then remove plating membrane by ion milling.
10. Repeat steps #1-10 for applying second layer of interconnect metal.

The plan to implement this new interconnect system consists of three phases. All three will be developed simultaneously before they are incorporated into the final 4 x 4 array circuit.

The first phase is to develop the improved planarization polyimide process. The major issues here are to obtain the PI-2556 polyimide material, optimize the curing process, and work out the etching parameters. The second phase is to develop the plating process. A gold plating system or an ion-milling tool will be utilized to improve the reliability of the metallic interconnection.

The work for the first two phases will be performed on dummy test wafers in order to optimize the process parameters. The third phase will be to use actual InP/InGaAs material to process 4 x 4 Active Pixel Arrays up to the component test part of the process. This way, qualified devices will be ready to go once the other two phases are successfully demonstrated.

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Currently the PI-2556 polyimide and related process chemicals are on order for the first phase of development. Samples will be demonstrated in a gold plating-ion milling process as the second phase development. For the third phase, 4 x 4 element Active Pixel Arrays will be processed.

The old process for depositing interconnects is as follows:[4]

1. Spin on planarization polyimide and cure.
2. Perform photolithography to open contact holes through polyimide.
3. Etch holes through polyimide.
4. Source, drain, and N-contact photolithography.
5. Electron Beam deposition of GeAuNiAu, lift-off, and anneal.
6. Gate and P-contact photolithography.
7. Electron Beam deposition of TiNiAu and lift-off.
8. Component probe test.
9. Interconnection #1 photolithography.
10. Electron Beam deposition of TiAu and lift-off.
11. Spin on passivation polyimide and cure.
12. Perform photolithography to open contact nodes through polyimide.
13. Etch holes through polyimide.
14. Interconnection #2 photolithography.
15. Electron Beam deposition of TiAu and lift-off.

Difficulties with properly controlling the etch depth through the polyimide layers without over-etching in some areas, coupled with the large steps that need to be traversed by the thin metal interconnect lines cause breaks and shorts in the lines, leading to poor yield.

IR FPA readout electronics will continue to benefit from continued DoD investment in IR FPAs. However, the technology is rapidly reaching a branch point. DoD IR FPAs are clustered in the atmospheric window wavelengths (3-5 μm, 8-12 μm) and are aimed at convenient operating conditions. These include 77-80 K operating temperature and video formats such as 640x480 for tactical applications. Some work continues in the longer wavelength, 20 K long wavelength detector area for space applications. However, scientific sensors require increasingly lower noise floors, with subelectron read noise desired by the end of this century. The need for large formats with long integration times increases the disparity between DoD-funded development and scientific requirements. To some extent, DoD is becoming more interested in infrared spectroscopy as a surveillance and reconnaissance technique so that some leverage may be expected in the future for the development of scientific infrared imaging spectroscopy instruments. These will be low noise, high data bandwidth instruments.

NASA's current needs in sensor electronics were identified. These needs include sub-electron read noise, cryogenic 4 K readout electronics for SIRTF, low noise discrete transistors for 80K, advanced packaging techniques (e.g. thermal compartmentalization), advanced interfaces such as analog-to-digital converters and optical links, and advanced architectures such as event-driven readout.

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otherwise, does not constitute or imply endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

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